Amendments to the Specification:

Please replace paragraph **[0003]** with the following amended paragraph:

[0003] The cross-section of the gate electrode 20 is in [[a]] the shape of a rectangle. Each of the gate insulation ~~layer~~ layers 40[[,]] and the amorphous silicon layer 50 has two opposite ~~incline~~ inclined surfaces. Each of the two phosphor-doped amorphous silicon layers 60a, 60b, the source electrode 70a, and the drain electrode 70b has an ~~incline~~ inclined surface.

Please replace paragraph **[0004]** with the following amended paragraph:

[0004] These ~~incline~~ inclined surfaces are produced in the process of ~~deposit~~ depositing, [[spray]] spraying or plating. [[But]] However, a coating with a flat surface is better for attaining [[a]] good ~~character of coating~~ characteristics. ~~So we do my best to flatten~~ Therefore it is desired that the ~~incline~~ inclined surfaces be as flattened as practicable.

Please replace paragraph **[0005]** with the following amended paragraph:

[0005] In a closed circuit composed of a resistance and a capacitance, [[a]] an RC (resistance-capacitance) delay is produced, which [[delay]] delays the signal transmission therein. For lowering the RC delay, the following two methods can be used ~~as follows:~~ . Firstly, ~~using~~ a low impedance material can be used to make the gate electrode 20~~, such as;~~ for example, Al, Cr, Ta, ~~its alloy, and so on;~~ or their alloys. Secondly, ~~increasing~~ the thickness and width of the gate electrode 20 can be increased to enlarge its ~~cross section~~ cross-sectional area. ~~Increasing~~ However,

increasing the width of the gate electrode 20 reduces the aperture ratio of the liquid crystal display, which lowers the light output efficiency. Furthermore, increasing the thickness of the gate electrode 20 makes the ~~incline~~ inclined surface steeper and lowers the ~~character~~ characteristics of the coating.

Please replace paragraph **[0007]** with the following amended paragraph:

[0007] In order to achieve the object set forth above, a TFT includes a substrate, a gate electrode disposed in the substrate, a gate insulation layer disposed on the substrate and gate electrode, a channel layer disposed on the gate insulation layer, a source ohmic contact layer and a drain ohmic contact layer arranged on opposite ends of the channel layer ~~and at the end of the channel layer~~, a source electrode disposed on the substrate and source ohmic contact layer, and a drain electrode disposed on the substrate and drain ohmic contact layer.

Please replace paragraph **[0008]** with the following amended paragraph:

[0008] Because [[of]] the gate electrode is disposed in the substrate, it is easy to increase the thickness of the gate electrode. In other words, it is easy to reduce the resistance of the gate electrode. [[So]] Thus the present invention can overcome the above described ~~disadvantage~~ disadvantages of the prior art.

Please replace paragraph **[0010]** with the following amended paragraph:

[0010] FIG. 1 is a ~~cross-section~~ cross-sectional view of a TFT according to the present invention[[;]].

Please replace paragraph **[0011]** with the following amended paragraph:

[0011] FIG. 2 is a ~~diagrammatic~~ top plan view of part of a display device using the TFT [[as]] shown in FIG. 1[[;]].

Please replace paragraph **[0012]** with the following amended paragraph:

[0012] FIG. 3 is a ~~cross-section~~ cross-sectional view of the display device [[as]] shown in FIG. 2[[;]].

Please replace paragraph **[0013]** with the following amended paragraph:

[0013] FIG. 4 to FIG. 9 ~~indicate~~ illustrate stages in the ~~processes~~ process of producing a gate electrode of the TFT [[as]] shown in FIG. 1[[;]].

Please replace paragraph **[0014]** with the following amended paragraph:

[0014] FIG. 10 to FIG. 13 ~~indicate~~ illustrate later stages in the ~~latter processes~~ process of manufacturing the TFT [[as]] shown in FIG. 1[[; ~~and~~]].

Please replace paragraph **[0015]** with the following amended paragraph:

[0015] FIG. 14 is a ~~cross-section~~ cross-sectional view of a conventional TFT.

Please replace paragraph **[0016]** with the following amended paragraph:

[0016] Referring to FIG. 1, ~~there~~ this is a ~~cross-section~~ cross-sectional view

of a TFT according to a first embodiment of the present invention. The TFT 200 includes a substrate 1, a gate electrode 2 disposed in the substrate 1, a gate insulation layer 4 disposed on the substrate 1 and the gate electrode 2, a channel layer 5 disposed on the gate insulation layer 4, a source ohmic contact layer 6a and a drain ohmic contact layer 6b arranged on two ends of the channel layer 5 respectively, a source electrode 7a disposed on the substrate 1 and the source ohmic contact layer 6a, and a drain electrode 7b disposed on the substrate 1 and drain ohmic contact layer 6b.

Please replace paragraph **[0017]** with the following amended paragraph:

[0017] ~~The surface of the gate electrode 2 is parallel with the surface of the substrate 1.~~ The substrate 1 can be made from glass or silicon oxide. The material of the gate electrode 2 can be [[metal]] a metallic conductive material, such as[[,]] Cu, Al, Ti, Mo, Cr, Nd, Ta, or ~~its alloy, and so on~~ alloys thereof. The gate insulation layer 4 can be made of silicon nitride or silicon oxide. The channel layer 5 can use amorphous silicon or polycrystalline silicon. The ohmic contact [[layer]] layers 6a and 6b can adopt amorphous silicon or phosphor-doped polycrystalline silicon. The surface of the gate electrode 2 is parallel with the surface of the substrate 1.

Please replace paragraph **[0018]** with the following amended paragraph:

[0018] Referring to FIG. 2, ~~there~~ this is a ~~diagrammatic~~ top plan view of part of a display device using the TFT 100 according to a second embodiment of the present invention. The gate electrode 2 is ~~contacted~~ in contact with a scanning line 17, [[and]] the source electrode 7a is ~~contacted~~ in contact with a signal line 18,

and the drain electrode 7b is ~~contacted~~ in contact with a pixel electrode 11. The gate electrode 2 receives a signal transported by the scanning line 17. A signal transported by the signal line 18 is received by the source electrode 7a, and then output by the drain electrode 7b to the pixel electrode 11. The pixel electrode 11 holds the potential depending on a storage capacitance (not shown) until the gate electrode 2 performs a next operation.

Please replace paragraph **[0019]** with the following amended paragraph:

[0019] Referring to FIG. 3, ~~there~~ this is a ~~cross-section~~ cross-sectional view of [[a]] the part of the display device [[as]] shown in FIG. 2. A protection layer 19 is formed on the thin film transistor. The pixel electrode 11 is formed on the protection layer 19 and drain electrode 7b. The storage capacitance comprises the pixel electrode 11, the gate insulation layer 4, the protection layer 19, and the scanning line 17. A color filter 14 and a black matrix 15 are formed on a substrate 16. A common electrode 13 is formed on the color filter 14 and the black matrix 15. A liquid crystal layer 12 is arranged between the pixel electrode 11 and the common electrode 13. The display device is driven by the TFT, so the display efficiency is ~~decided~~ determined by the potential of the pixel electrode 11.

Please replace paragraph **[0020]** with the following amended paragraph:

[0020] Because [[of]] the gate electrode 2 is deposited in the substrate 1, the thickness of the gate electrode 2 can be changed [[with]] by changing the depth of the substrate 1 etched. Thus it is easy to increase the thickness of the gate electrode 2 to reduce [[the]] its impedance. Furthermore, the height of the gate electrode 2 can be almost [[be]] equal to that of the substrate 1. Therefore, the

TFT 100 can efficiently reduce [[a]] an RC delay of a scanning signal.

Please replace paragraph **[0021]** with the following amended paragraph:

[0021] A method of producing the thin film transistor [[as]] shown in FIG. 1 comprises: a photo mask process of producing the gate electrode 2, and a ~~latter processes~~ later process of manufacturing the thin film transistor.

Please replace paragraph **[0022]** with the following amended paragraph:

[0022] The photo mask ~~processes~~ process of producing the gate electrode 2 is shown in FIG. 4 to FIG. 9, and comprises the following ~~have~~ steps ~~as follows~~:

Firstly, as shown in FIG. 4, coating a photo-resist film 8 on a substrate 1, and baking the photo-resist film 8[[;]].

Secondly, as shown in FIG. 5, using an ultraviolet light to expose the photo-resist film 8 through a photo mask having a predetermined pattern by way of projection ~~manner~~, and then forming a pattern by developing[[;]].

Thirdly, as shown in FIG. 6, forming a slot 2a on the substrate 1 by ~~method~~ way of dry etching or wet etching[[;]].

Fourthly, as shown in FIG. 7, ~~wiping off~~ removing the residual ~~of the~~ photo-resist film 8 by ~~a method~~ way of dissolving, oxidizing, or directly peeling off[[;]] the residual photo-resist film 8.

~~And then~~ Fifthly, as shown in FIG. 8, depositing a metal layer 3 on the substrate 1 to fill the slot 2a[[;]].

Lastly, as shown in FIG. 9~~, wiping off~~, removing the metal on the substrate 1 by polishing to form a gate electrode 2, [[and]] the gate electrode 2 [[fills]] filling the slot 2a.

Please replace paragraph **[0023]** with the following amended paragraph:

[0023] Some changes can be made [[in]] to the ~~former~~ above-described process of producing the gate electrode 2. ~~Such as~~ For example:
1. ~~omitting the~~ The step of ~~wiping off~~ removing the residual ~~of the~~ photo-resist film 8, as shown in FIG. 7, ~~directly depositing~~ can be omitted. Instead, the metal layer 3 can be directly deposited on the substrate 1 and the photo-resist film 8[[,]]. ~~and then wiping off~~ Then the photo resist film 8 can be removed to form the gate electrode 2;
2. ~~the~~ The photo-resist film 8 can be formed on the metal layer 3[[,]] using an ultraviolet light to expose the photo-resist film 8 through a photo mask having a predetermined pattern by way of projection ~~manner~~, and then ~~forming~~ a pattern can be formed by developing[[,]]. ~~wiping off~~ Then the metal around the slot 2a and the photo-resist film 8 can be removed to form the gate electrode 2.

Please replace paragraph **[0024]** with the following amended paragraph:

[0024] The ~~latter processes~~ later process of producing the thin film transistor is shown in FIG. 10 to FIG. 13 and in FIG. 1.

Please replace paragraph **[0025]** with the following amended paragraph:

[0025] [[First]] Firstly, as shown [[as]] in FIG. 10, ~~using~~ chemical vapor deposition (CVD) is used to ~~forming~~ form the gate insulation layer 4, wherein the reaction gases are silicon alkyl and ammonia. ~~And then using a method of~~ Then a CVD method is used to ~~forming~~ form an amorphous silicon layer 9 on the

insulation layer 4, wherein the reaction gases are silicon chloride and hydrogen. After that, ~~forming~~ a phosphor doped amorphous silicon layer 6 is formed on the amorphous silicon layer 9 by doping technology.

Please replace paragraph **[0026]** with the following amended paragraph:

[0026] ~~Second~~ Secondly, as shown [[as]] in FIG. 11, [[using]] a photo mask process is used to etch two sides of the amorphous silicon layer 9 and the phosphor doped amorphous silicon layer 6 ~~till showing up~~ until the gate insulation layer 4 is reached.

Please replace paragraph **[0027]** with the following amended paragraph:

[0027] ~~Third~~ Thirdly, as shown [[as]] in FIG. 12, ~~depositing~~ a source and drain metal layer 7 is deposited on the phosphor amorphous layer 6 and the gate insulation layer 4.

Please replace paragraph **[0028]** with the following amended paragraph:

[0028] ~~Subsequently~~ Fourthly, as shown [[as]] in FIG. 13, [[using]] a photo mask process is used to etch the middle area of the source and drain metal layer 7 ~~till showing up~~ until the amorphous silicon layer 6~~, and then~~ is reached, thereby forming a source electrode 7a and a drain electrode 7b.

Please replace paragraph **[0029]** with the following amended paragraph:

[0029] [[Last]] Lastly, ~~wiping off~~ the middle area of the phosphor doped

amorphous silicon layer 6 is removed by ~~a method~~ way of dry etching, ~~and then~~ thereby forming a gate ohmic contact layer 6a, a drain ohmic contact layer 6b and a channel layer 5. That is, the TFT 100 as shown in FIG. 1 is produced.

Please replace paragraph **[0030]** with the following amended paragraph:

[0030] ~~And the section~~ The sectional shape of the gate electrode 2 is ~~not only trapezoid,~~ trapezoidal. ~~further, its section shape is also rectangle~~ Alternatively, the sectional shape may be rectangular.